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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,507	07/24/2003	Son Ho	MP0390	1965

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EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,507	HO ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/24/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-120* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-43,70-78 and 112-120* is/are allowed.

6)☒ Claim(s) *1-11,13-15,20-28,30-31,44-50,52-54,59-63,65-66,79-89,91-93,97-105,107-108* is/are rejected.

7)☒ Claim(s) *12,16-19,29,32-34,51,55-58,64,67-69,90,94-96,106 and 109-111* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/5/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. For example the designation numbers for host and servo CPUs are not matching with drawing of figure 2 on page 8 of specification. Applicant's cooperation is requested in correcting similar errors throughout the length of the specification.

Claim Objections

3. Claims 2 and 3 are objected to because of the following informalities:

As per claims 2 and 3, acronyms (such as RAM in claim 2) should not be used to abbreviate key phrases until they are explicitly defined previously within the claim, or in a claim to which it depends. An example of an accepted correction would be "random access memory (RAM)".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 11,13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91-93, AND 97 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Zaidi et al. (US 6,601,126 B1) (Zaidi herein after) and Jim Handy (The Cache Memory Book, second edition, published 1998) (Jim herein after submitted as evidentiary reference).

As per claims 1, 44 and 79, Zaidi teaches a cache control system (fig. 1) that controls data flow between a line cache (fig, 1, item 126), a first central processing unit (CPU) (fig. 1, item 110) and first and second memory devices (fig. 1, items 106 and 108), comprising:

a first line cache interface that is associated with the first CPU (taught as cache and channel controller interface the CPU bus, column 4, lines 39-41), that receives a first program read request from CPU and that generates a first address from said first program read request (column 23, lines 30-32);

a first memory interface that communicate with first memory device and second memory interface that communicates with the second memory device (fig. 1, items 106 and 108, two memory devices are connected to memory bus through arbiter, which inherently teaches first and second interfaces connected to first and second memory devices);

a cache (fig. 1, item 126); and a switch that selectively connects said line cache to one of said first and second memory interfaces (column 23, lines 41-45),

Zaidi fails to teach line cache receiving first address and comparing address to stored addresses and if match occurs it returns data to CPU, and retrieves data from

one of the first and second memories if miss occurs. Zaidi teaches a system with cache memory and it is well known to one of ordinary skill in the art at the time of invention that when CPU issues read request, cache compares the address with the stored addresses and returns the data to CPU and if miss occurs it retrieves data from higher latency storages (see Jim, page 42-43, section 2.1.3) (also applicant's admitted prior art in the background of the invention section).

As per claims 2-3, 45-46 and 80-81, Zaidi teaches that the first memory device is RAM (fig. 1, item 108).

As per claims 4, 47 and 82, second memory device is flash memory (fig. 1, item 106).

As per claim 5, 48 and 83, first CPU is an advanced risc machine (ARM) processor (column 5, lines 35-36).

As per claims 11, 50 and 89, Zaidi teaches a cache memory as per claim 1 and memories are used for storing data. Zaidi fails to teach cache with a Content Addressable Memory (CAM). Jim teaches a cache memory with CAM, which stores addresses associated with data stored in the cache memory (page 14, sec. 1.5, page 15, fig. 1.7). Jim teaches cache determines when hit and miss occurs and retrieves data from higher latency memories (first and second memories) when miss occurs (pages 42-43, sec. 2.1.3 and pages 46-47, fig. 2.4). Thus Jim inherently teaches cache state machine.

It would have been obvious to one having ordinary skill in the art at the time of invention have used Zaidi's dual processor system and modified to use the cache with

CAM as taught by Jim because CAM permits content of memory to be searched and matched instead of having to specify a memory location in order to retrieve data from memory (page 14, sec. 1.5). This allows data to be stored at any location in a cache (page 16, paragraph 3)

As per claims 13-14, 52-53 and 91-92, Jim teaches a cache replacement algorithm Least Used Page, which replaces least used page with data retrieved form the first or second memory when miss occurs (page 57, paragraph 2). Thus Jim inherently teaches least used page device.

As per claims 15, 54 and 93, Jim teaches that state transitions of cache state machine are based, in part on at least one internal state of the CPU (page 42, paragraph 2 and 3 and sec. 2.1.3)

As per claims 20 and 97, Jim teaches that cache can have many ways of implementations depending upon the depending upon the address bits used in the system (page 54, paragraphs 2 and 3). Thus Jim inherently teaches cache with 4 pages of 8 x 32.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-10, 49, 84-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi and Jim Handy as applied to claims 1-5 above, and further in view of Barroso et al. (US 6,725,334 B2).

As per claims 6, 49 and 84, Zaidi and Jim teach a dual processor system with two caches (fig. 2, items 202 and 214, first and second processors, and items 208 and 224, two caches). Zaidi and Jim inherently teach cache interface with first and second CPUs and both generates read requests and hence first and second address as taught in claim 1. Zaidi teaches system with two caches for two processors and Zaidi fails to teach cache arbitration device which communicates with first and second cache interfaces and resolves cache access conflicts between first and second CPUs. Barroso teaches a second level cache with switch (fig. 1, item 130 and 120), which provides interfaces with first and second CPU and arbitrates between first and second CPU (column 4, lines 10-21).

It would have been obvious to one having ordinary skill in the art at the time of invention would have modified the multiple cache with multiple processor system of Zaidi and used one cache with switch as taught by Barroso to reduce the cost and the waste of the cache capacity (column 1, lines 45-65).

As per claims 7-8 and 85-86, Zaidi and Barroso fail to teach direct interfaces from processors to memory devices. Jim teaches that a designer will allow the CPU address to propagate directly to main memory (page 44, paragraph 2). Thus Jim inherently teaches a direct memory interface from CPU to memory.

It would have been obvious to one having ordinary skill in the art at the time of invention would have used the direct memory interface as taught by Jim in the systems of Zaidi and Barroso to reduce the time to retrieve the data from main memory in case of miss occurs in the cache (page 44, paragraph 2).

As per claims 9 and 87, Zaidi and Barroso teach an arbiter (Zaidi, fig. 2, item 244) and switch (Barroso, fig.1, item 120) to resolve memory access conflict (Zaidi, column 23, lines 40-45).

As per claims 10 and 88, Zaidi teach an application specific integrated circuit (ASIC) which can be used to provide interconnection structure and method for efficient integration variety functional circuits (column 2, lines 63-65). It would have been obvious to one having ordinary skill in the art at the time of invention have used the embedded system of Zaidi to control the hard disk drive and its components for better performance and compact design.

Claims 21-28, 30-31, 59-63, 65-66, 98-105,107-108 are rejected under same rationale as applied to claims 1-5, 11, 13-15, and 6-10 as above.

Allowable Subject Matter

8. Claims 12,16-19, 29, 32-34, 51, 55-58, 64, 67-69, 90, 94-96, 106 and 109-111 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 35-38, 39-43, 70-73, 74-78, 112-115 and 116-120 are allowed.

10. The following is an examiner's statement of reasons for allowance:

As per independent claims 35, 70 and 112, Zaidi, Barroso and Jim fail to teach a cache line system or method which selects first and second least used pages when miss occurs and replaces one of first and second least used page based on internal state of first CPU.

As per claims 39, 74 and 116, Zaidi, Barroso and Jim fail to teach a cache line system or method which allows one of pages from cache to be accessed by one of the first and second processors while the other of the first and second processors is waiting for data retrieval to another of pages when miss occurs in the cache.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

11. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Borkenhagen et al. (6,151,664) teaches a programmable cache interface which supports SRAM and DRAM as cache.

Rodriguez et al. (US 2003/0217230 A1) teaches a method to avoid cache flooding using least recently used page algorithm when miss occurs in the cache.

Byers et al. (US 2204/0199718 A1) a system for embedded disk controller using main processor and servo controller that is coupled to a second processor. The second processor may be a digital signal processor that is operationally coupled to the first main processor through an interface.

Elnathan et al. (US 6,820,170) teaches a CAM based cache structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

12/9/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER